**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1–7 (canceled)

Claim 8 (new). An ingress/egress port for an Ethernet switch. comprising:

a plurality of MAC interfaces, each MAC interface is capable of receiving/transmitting FE packets, at least one of the MAC interfaces further being configurable to receive/transmit GE packets; and

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit GE and FE packets to, the interfaces.

Claim 9 (new). The port according to claim 8 wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, the other MAC interfaces only being adapted to receive/transmit FE packets.

Claim 10 (new). The port according to claim 9 wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 11 (new). The port according to claim 8 wherein which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 12 (new). The port according to claim 8 wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 13 (new). The port according to claim 12, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 14 (new). The port according to claim 13, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 15 (new). The port according to claim 13, wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory.

Claim 16 (new). A port according to claim 8 wherein the plurality of MAC interfaces consists of 8 MAC interfaces.

Claim 17 (new). An Ethernet switch comprising:

An ingress/egress port for an Ethernet switch having

a plurality of MAC interfaces, each MAC interface is capable of receiving/transmitting FE packets, at least one of the MAC interfaces further being configurable to receive/transmit GE packets, and

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit GE and FE packets to, the interfaces;

at least one other ingress/egress port.

Claim 18 (new). The Ethernet switch according to claim 17, wherein each of the other ingress/egress ports comprises:

a plurality of MAC interfaces, each MAC interface capable of receiving/transmitting FE packets, at least one of the MAC interfaces further being configurable to receive/transmit GE packets; and

receive and transmit modules which are configurable respectively to receive both GE and FE packets from, and transmit GE and FE packets to, the interfaces.

Claim 19 (new). The Ethernet switch according to claim 18, wherein the ingress/egress port and the other ingress/egress ports total eight ingress/egress ports, each ingress/egress port being switchable between two modes, a first mode operating as one GE port and a

second mode operating as eight FE ports, and wherein the switch can operate as *n* GE ports and 8(8-*n*) FE ports.

Claim 20 (new). The Ethernet switch according to claim 17, wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 21 (new). The Ethernet switch according to claim 20, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further operable to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 22 (new). The Ethernet switch according to claim 21, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 23 (new). The Ethernet switch according to claim 21, wherein the receiver interface is further operable to store the descriptor associated with the packet data in the memory.

Claim 24 (new). A method, comprising

providing data packets to an ingress/egress port, the ingress/egress port having a plurality of MAC interfaces each of which is capable of receiving/transmitting FE

packets, at least one of the MAC interfaces further being configurable to receive/transmit GE packets; and

passing packet data from the data packets from the ingress/egress ports to one or more receive modules, the one or more receive modules configurable to receive both GE and FE packets; and

passing outgoing packet data from one or more transmit modules to the ingress/egress port, the one or more transmit modules configurable to transmit both GE and FE packets.

Claim 25 (new). The method according to claim 24, further comprising providing a control signal to the ingress/output port to determine whether the MAC interfaces operate as FE interfaces or whether the at least one interface operates as a GE interface.

Claim 26 (new). The method according to claim 25, wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.

Claim 27 (new). The method according to claim 24, wherein only one of the MAC interfaces is configurable to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.